In the Claims:

1.   (Currently Amended)   A method for operating a pipeline in a processor comprising;

fetching a number of <u>unfused</u> instructions<u>, said number of fetched unfused instructions being</u> greater than the number of execution units in a processor, and

combining a plurality of <u>the fetched unfused</u> instructions into a control word which can be processed by one execution unit.

2.   (Currently Amended) The method according to Claim 1 wherein:

two <u>of the fetched unfused</u> instructions are combined into a control word.

3.   (Original) The method according to Claim 1 further comprising;

issuing the control word to an execution unit.

4.   (Currently Amended) The method according to Claim 1 wherein;

said processor has four execution units and said pipeline fetches at least five <u>unfused</u> instructions.

5.   (Currently Amended) The method according to Claim 4 wherein;

said pipeline fetches eight <u>unfused</u> instructions.

6.   (Original) The method according to Claim 4 wherein;

said pipeline checks instructions for conflicts and issues valid control words to said execution units.

7.   (Original) The method of Claim 6 wherein;

said pipeline issues control words to all four execution units.

8.   (Currently Amended) A processor comprising:

an instruction pipeline having a first stage ~~fetching and decoding~~ which fetches and decodes a number of unfused instructions, the number of unfused instructions fetched and decoded by said first stage being greater than the number of execution units in said processor, and

fusing logic in a second stage of said pipeline combining a plurality of said decoded unfused instructions into a control word which can be executed by one execution unit.

9.   (Original) The processor of Claim 8 further including;

an issue slot in said second stage for coupling said control word to following stages of said pipeline.

10.   (Original) The processor of Claim 9 further including;

an execution unit in a third stage of said pipeline receiving and executing the control word.

11.   (Currently Amended) The processor of Claim 8 wherein;

said processor comprises four execution units and said first pipeline stage fetches at least five <u>unfused</u> instructions.

12.   (Currently Amended) The processor of Claim 11 wherein;

said <u>first</u> pipeline <u>stage</u> fetches eight <u>unfused</u> instructions.

13.   (Currently Amended) The processor of Claim 8 further comprising;

grouping logic in said second stage checking said <u>unfused</u> instructions for conflicts and issuing only valid control words.

14.   (Original) The processor of Claim 13 wherein;

said processor comprises four issue slots receiving valid control words.

15.   (Original) The processor of Claim 14 wherein;

said processor issues control words to all four execution units in one clock cycle.

16.   (Original) The processor of Claim 14 wherein said processor comprises;

four execution units, each receiving control words from one of said issue slots.

17.   (Currently Amended)   A system for coupling instructions from memory to execution units in a processor comprising;

fetching means for fetching and decoding a number of <u>unfused</u> instructions, the number of unfused instructions fetched and decoded by said fetching means being greater than the number of execution units in said processor, and

fusing means for combining a plurality of said <u>fetched and decoded unfused</u> instructions into a control word which can be executed by one execution unit.

18.   (Original) The system of Claim 17 further comprising;

grouping means for checking said <u>fetched and decoded unfused</u> instructions for conflicts which would prevent simultaneous execution of said instructions.

19,   (Original) The system of Claim 18 further comprising;

issue means for issuing control words which may be executed simultaneously to a plurality of said execution units.

20.   (Original) The system of Claim 19 wherein;

said processor comprises four execution units and

said issue means includes slots for issuing a control word to each execution unit.

21.   (Currently Amended) The system of Claim 20 wherein;

said fetching means fetches eight <u>unfused</u> instructions simultaneously.

22.   (New) The method according to Claim 1, wherein combining a plurality of unfused instructions into a control word which can be processed by one execution unit further comprises:

combining, into said control word, a plurality of non-conflicting unfused instructions capable of being executed simultaneously.

23.   (New) The method according to Claim 1, wherein combining a plurality of unfused instructions into a control word which can be processed by one execution unit further comprises: .

combining, into said control word, a plurality of conflicting unfused instructions incapable of being executed simultaneously.

24.   (New) The method according to Claim 1, wherein combining a plurality of unfused instructions into a control word which can be processed by one execution unit further comprises:

combining, into said control word, a plurality of unfused instructions, each of which modifies a common register.

25.   (New) The method according to Claim 1, and further comprising:

returning unfused instructions which cannot be combined and processed by one execution unit;

wherein said returned unfused instructions are included in a next fetching of a number of unfused instruction greater than the number of execution units in a processor.

26.   (New) The processor of Claim 8, wherein said fusing logic in said second stage of said pipeline further comprises grouping and fusing logic for combining, into said control word, a plurality of non-conflicting unfused instructions capable of being executed simultaneously.

27.   (New) The processor of Claim 8, wherein said fusing logic in said second stage of said pipeline further comprises grouping and fusing logic for combining, into said control word, a plurality of conflicting unfused instructions incapable of being executed simultaneously.

28.   (New) The processor of Claim 8, wherein said fusing logic in said second stage of said pipeline further comprises grouping and fusing logic for combining, into said control word, a plurality of unfused instructions, each of which modifies a common register.

29.   (New) The system of Claim 17, wherein said fusing means further comprises:

grouping and fusing means for combining, into said control word, a plurality of non-conflicting unfused instructions capable of being executed simultaneously.

30.   (New) The system of Claim 17, wherein said fusing means further comprises:

grouping and fusing means for combining, into said control word, a plurality of conflicting unfused instructions incapable of being executed simultaneously.

31.   (New) The system of Claim 17, wherein said fusing means further comprises:

grouping and fusing means for combining, into said control word, a plurality of unfused instructions, each of which modifies a common register.

32.   (New) The system of Claim 28, and further comprising:

return means for returning unfusible instructions to said memory;

said fetching means fetching and decoding said returned unfusible instructions in a next fetch from said memory.